ABSTRACT OF THE DISCLOSURE

A behavioral synthesis system is provided, which comprising a section for generating a control data flow graph from a behavioral description containing a loop process and a non-loop process, using nodes representing processing sections and input/output branches representing data flow, and a section for automatically synthesizing hardware structure at a register transfer level using the control data flow graph. A loop process portion of the control data flow graph represents that the nodes contained in the loop process are divided into pipelined stages and processes of the pipelined stages are executed in parallel in each of a plurality of the loop processes. The control data flow graph generating section comprises, in the loop process portion, a loop control portion for outputting control signals for executing at least the non-loop process of the loop process and the non-loop process, to the nodes in the stages.